

FIG. 1 (Prior Art)

FIG. 2 (Prior Art)

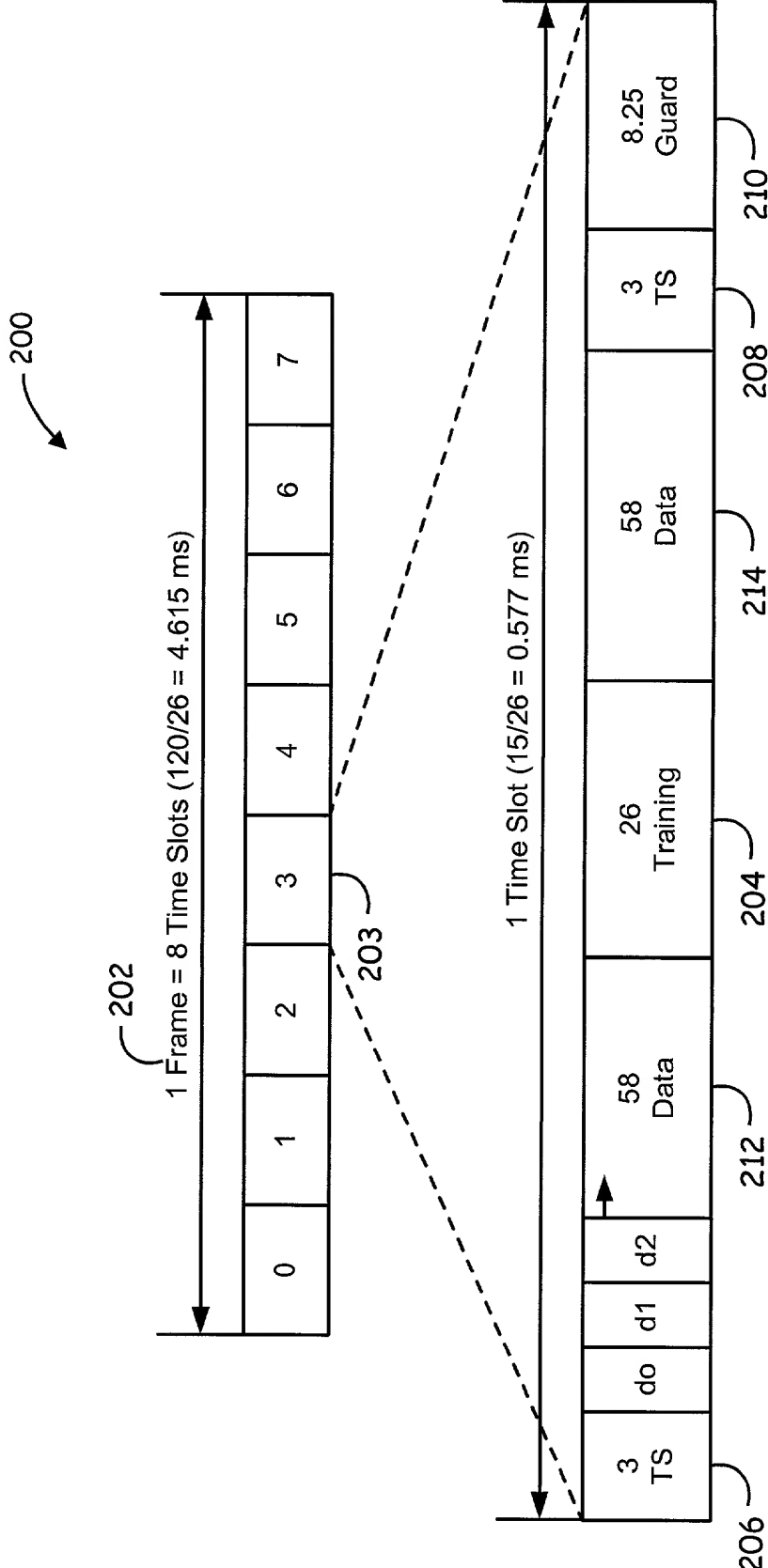


FIG. 2 (Prior Art)

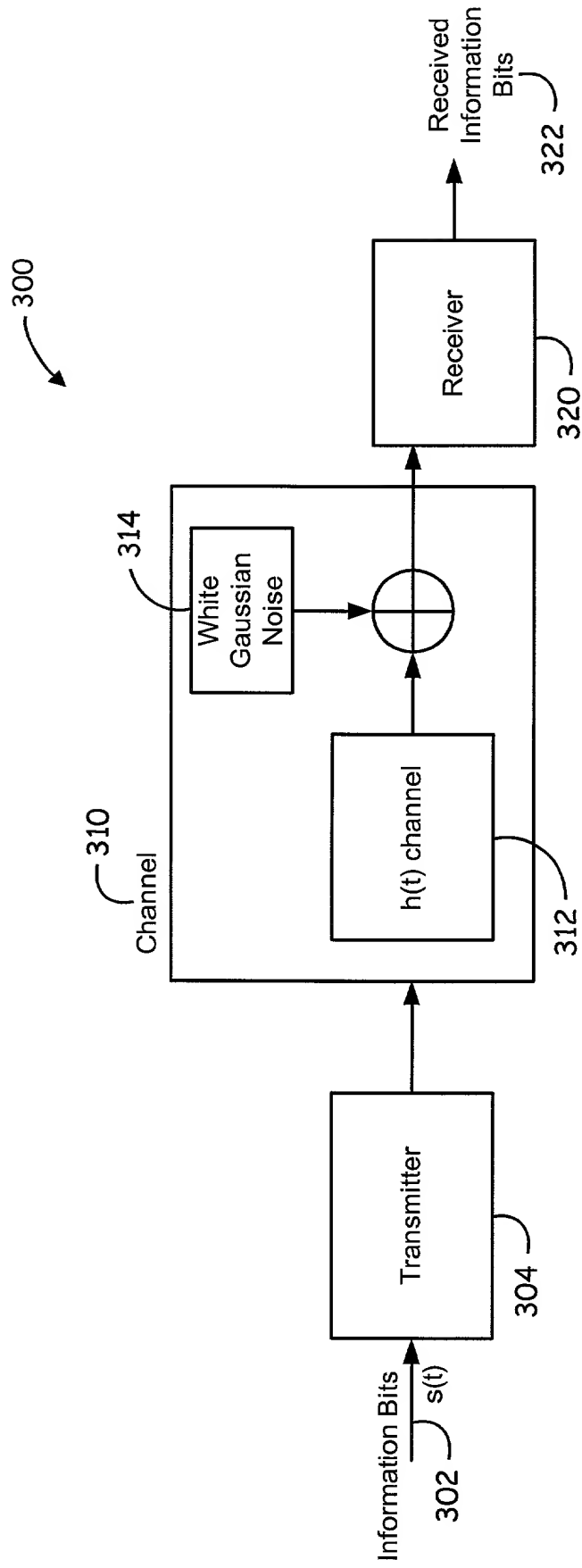


FIG. 3 (Prior Art)

FIG. 4 is a block diagram of a communication system 400. The system 400 includes a Frame Formatting block 402, a Channel Encoding and Puncturing block 404, an Interleaver block 406, a Burst Builder block 408, and a Modulator block 410. The blocks are connected in a sequential manner, with data flowing from left to right. The Frame Formatting block 402 outputs to the Channel Encoding and Puncturing block 404, which outputs to the Interleaver block 406. The Interleaver block 406 outputs to the Burst Builder block 408, which outputs to the Modulator block 410. The Modulator block 410 outputs to an antenna, represented by a circle with a dot in the center.

400

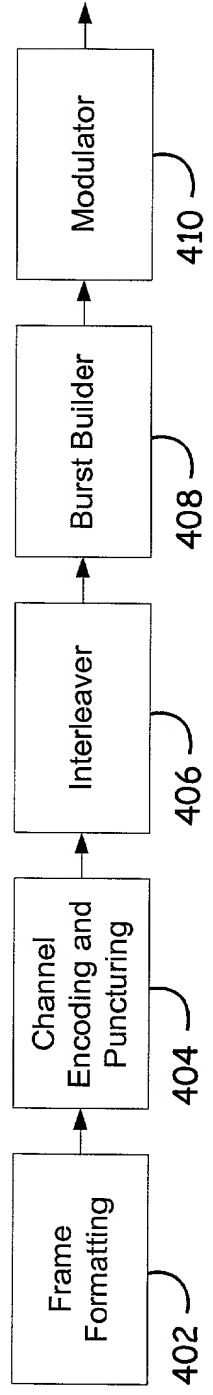


FIG. 4

FIG. 5

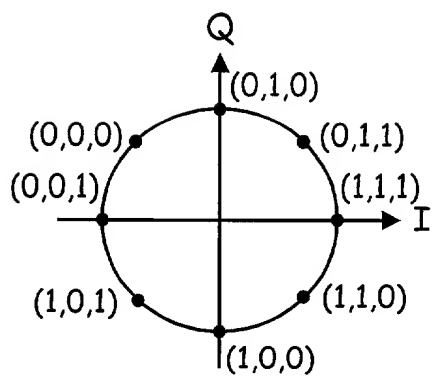


FIG. 5

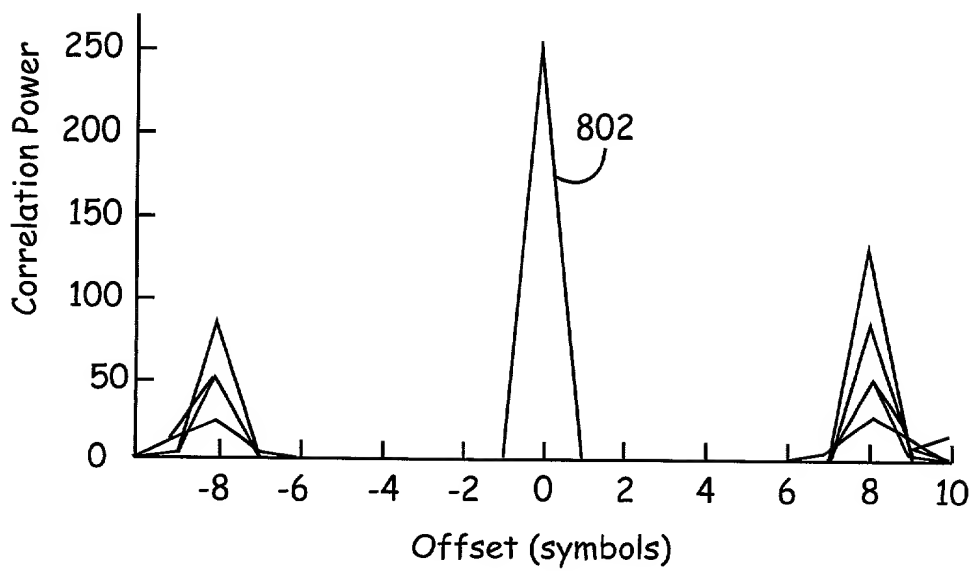


FIG. 8

FIG. 9 is a block diagram of a DFE system 900. The system includes a Feed Forward Filter 902, a Decision Process 908, and a FeedBack Filter 904. The system also includes a set of taps 903 with coefficients h_0, h_1, h_2, h_3 . The system is labeled 900.

DFE

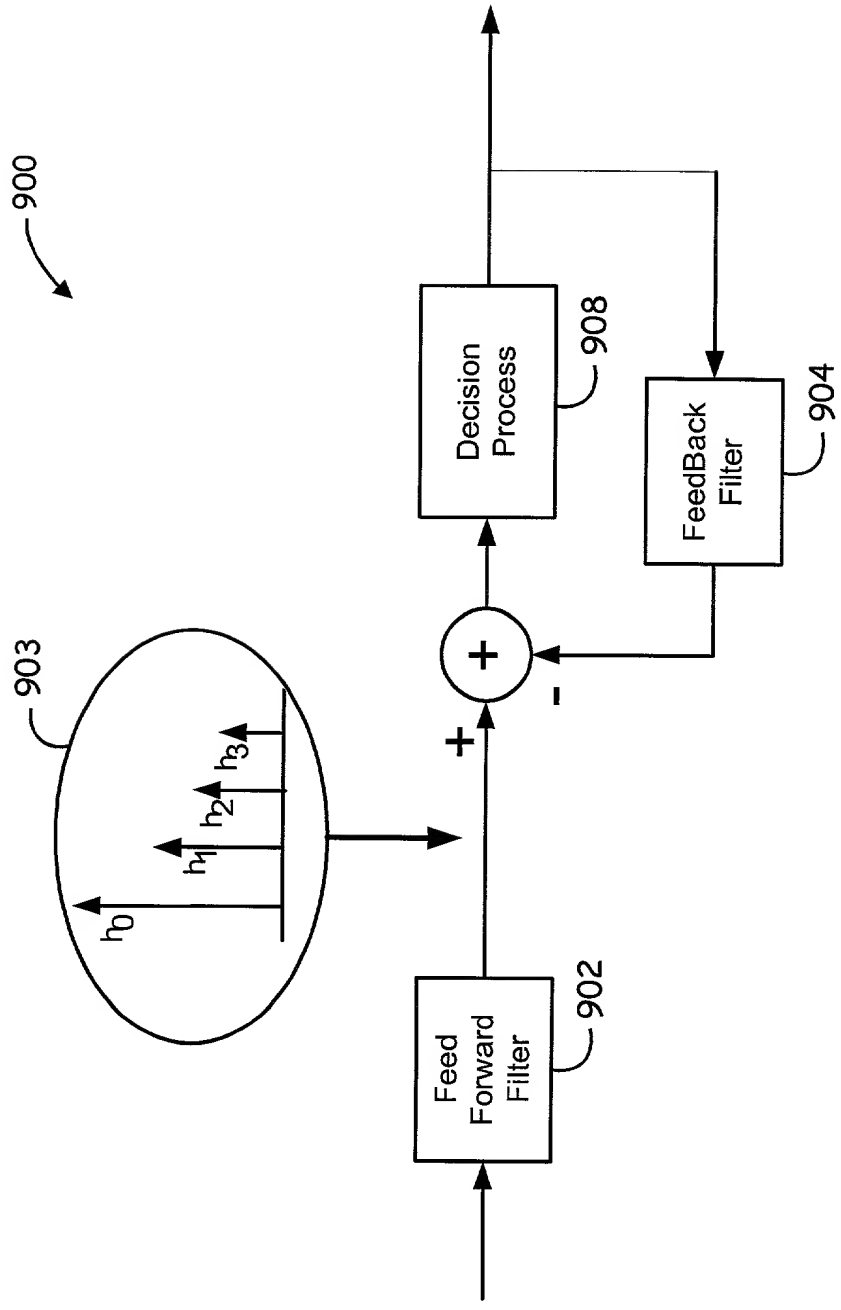


FIG. 9 (Prior Art)

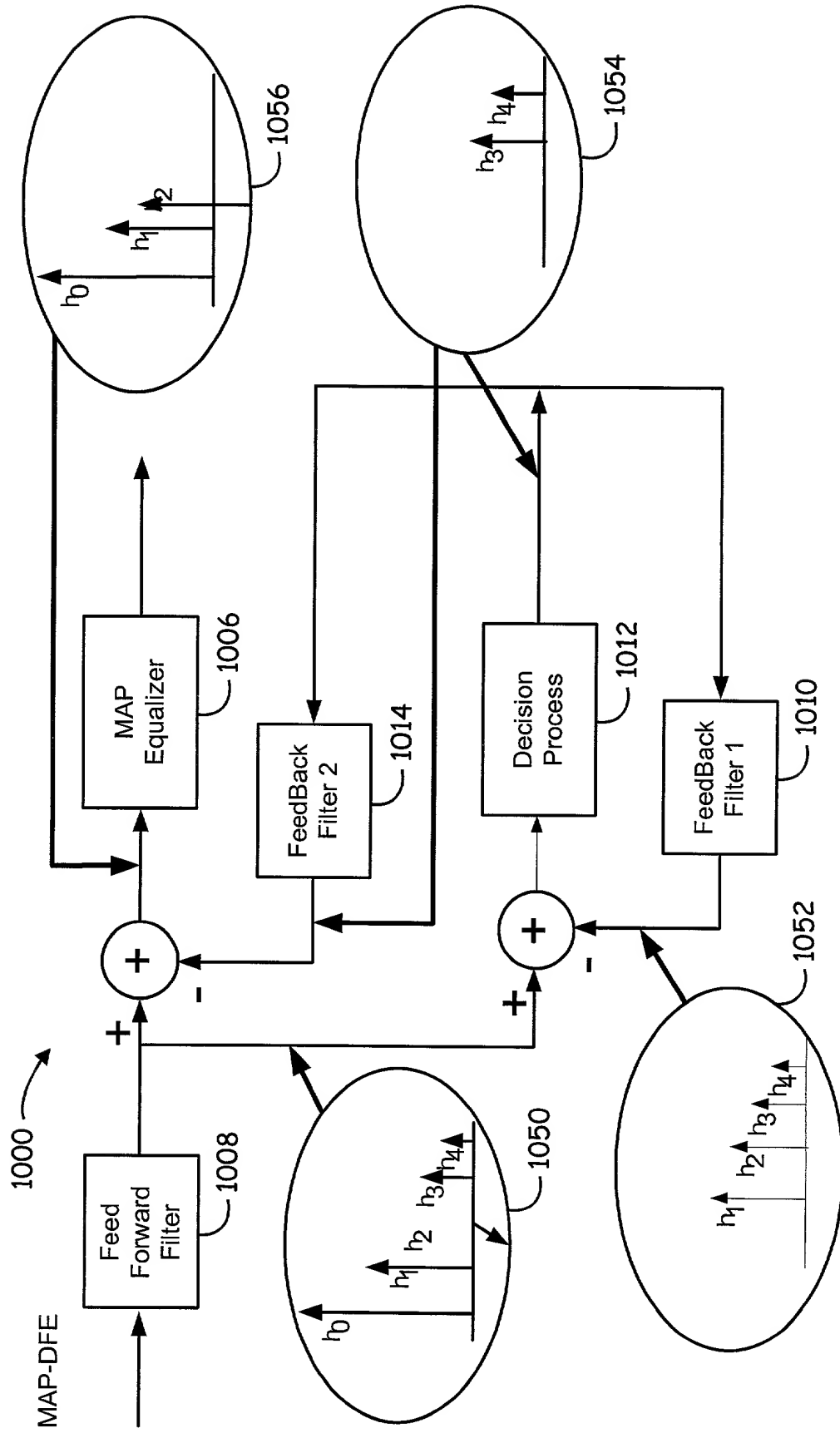


FIG. 10 (Prior Art)

FIG. 11 is a block diagram of a channel model 1100. The channel model 1100 includes a channel 1102 with taps h_0, h_1, h_2, h_3, h_4 . The channel 1102 is connected to a modulation block 1104 with modulation M . The equalizer complexity (States) is M^L .

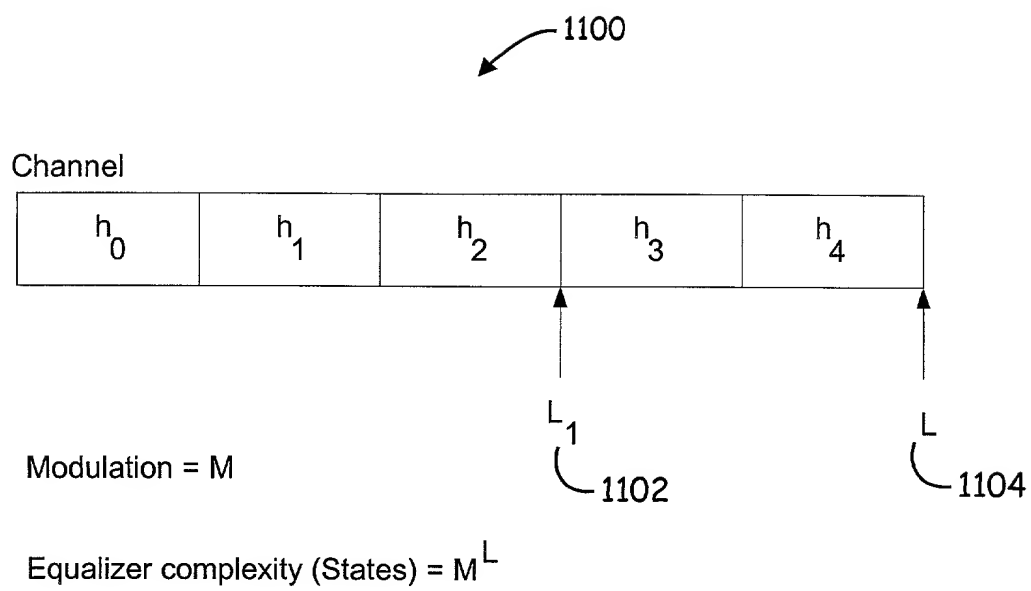


FIG. 11

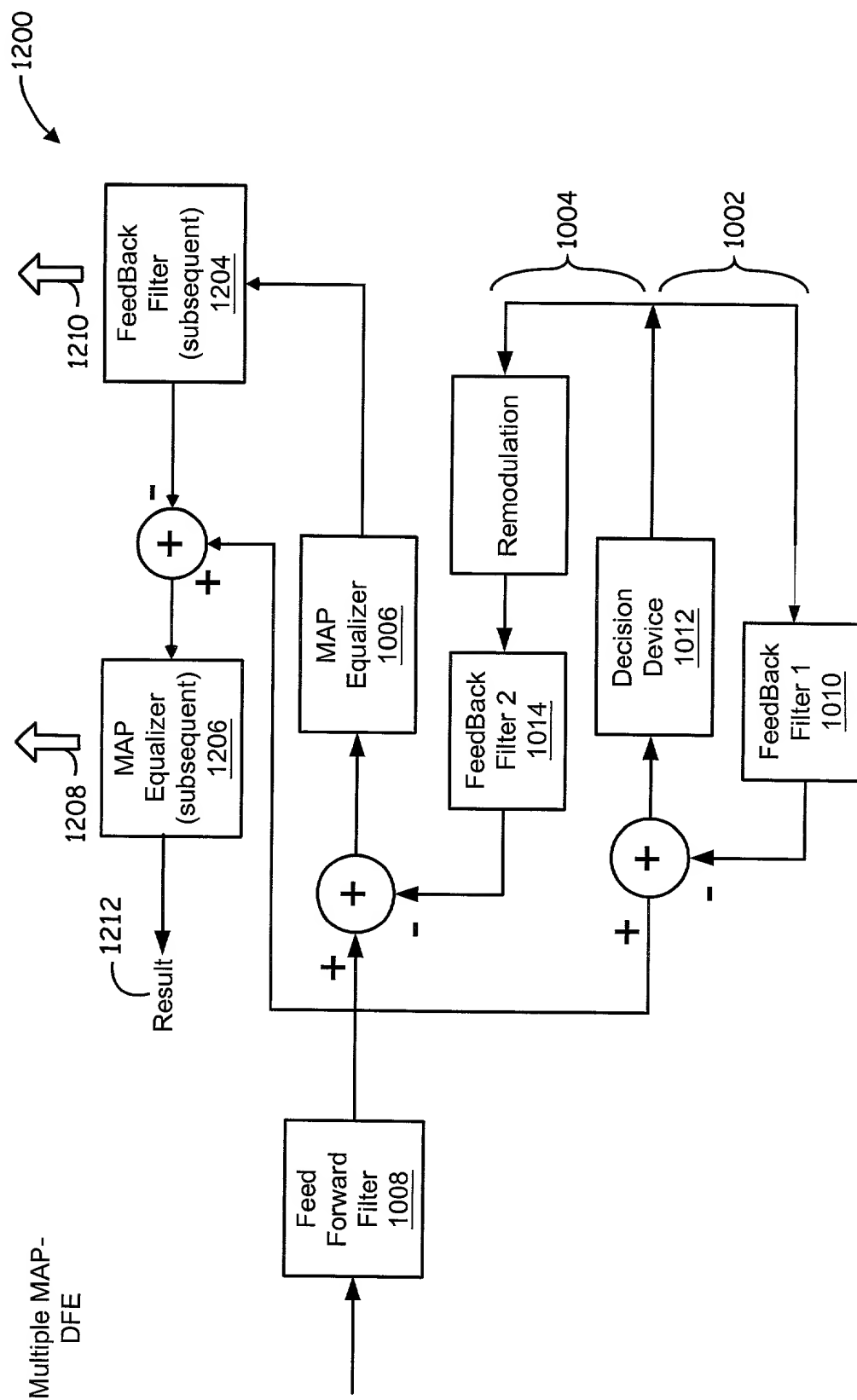


FIG. 12

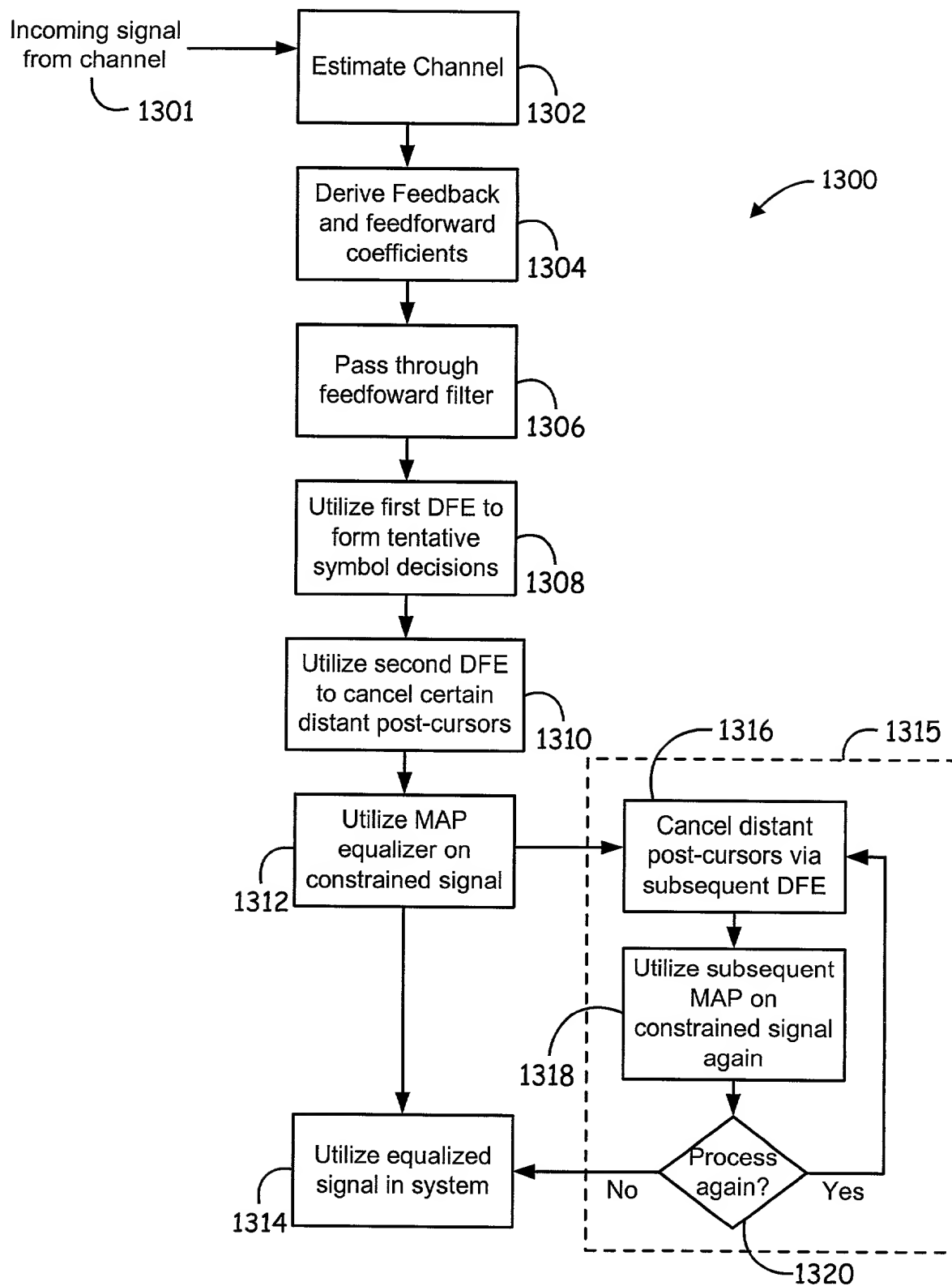


FIG. 13